EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	22	(second near (organosilicate or OSG)) and ((Silicon near oxide) or SiO or "SiO.sub.2")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/02 07:52
L2	1216	(organosilicate or OSG or organo$6) and damascene	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/02 07:50
L3	2401	(fluorocarbon or fluorine or "CHF.sub. 3" or "CH.sub.2F.sub.2 or ""CH.sub. 3F"" or ""CF.sub.4"" or ""C.sub.2F.sub. 6") near8 (etch or etching or etchant or etched) near8 (trench or trenches or via or vias or hole or opening or openings)	US-PGPUB; USPAT; USOCR	OR	ON	2006/08/02 07:50
L4	134	L2 and L3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/02 07:50
L5	404964	(SiO or "SiO.sub.2" or "SiO.sub.x" or "SiO.sub.n" or (silicon near oxide))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/02 07:50
L6	110	L4 and L5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/02 07:50
L7	44	L6 and ((@ad<"20010202") or (@rlad<"20010202"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/02 07:50
L8	2	("6410437").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/02 07:50

EAST Search History

L9	5	("5817572" | "5970336" | "6030901" | "6072227" | "6168726").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/08/02 07:50

US006072227A

United States Patent [19]

Yau et al.

[11] Patent Number: 6,072,227

[45] Date of Patent: Jun. 6, 2000

[54] **LOW POWER METHOD OF DEPOSITING A LOW K DIELECTRIC WITH ORGANO SILANE**

[75] Inventors: **Wai-Fan Yau**, Mountain View; **David Cheung**, Foster City; **Shin-Puu Jeng**, Cupertino; **Kuowei Liu**, Santa Clara; **Yung-Cheng Yu**, San Jose, all of Calif.

[73] Assignee: **Applied Materials, Inc.**, Santa Clara, Calif.

[21] Appl. No.: **09/114,682**

[22] Filed: **Jul. 13, 1998**

Related U.S. Application Data

[63] Continuation of application No. 09/021,788, Feb. 11, 1998.

[51] **Int. Cl.**[7] **H01L 23/58**

[52] **U.S. Cl.** **257/642**; 257/635; 257/636; 257/640

[58] **Field of Search** 257/635, 636, 257/640, 642, 647, 648

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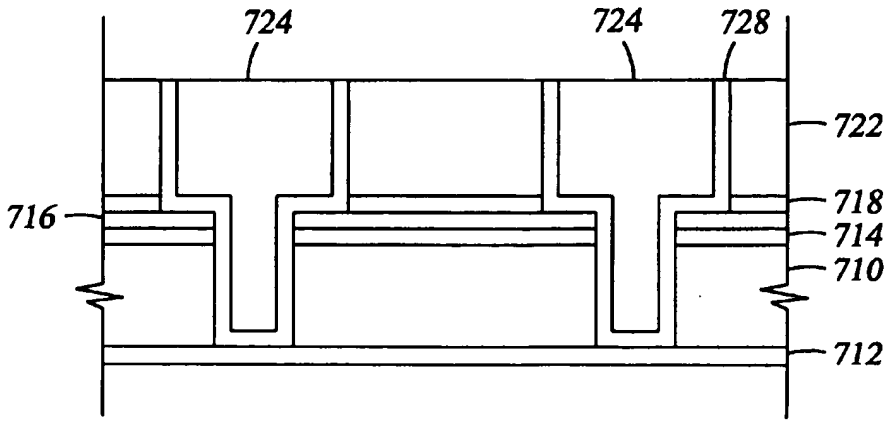
Primary Examiner—Mahshid Saadat
Assistant Examiner—Allan R. Wilson
Attorney, Agent, or Firm—Thomason, Moser & Patterson

[57] **ABSTRACT**

A method and apparatus for depositing a low dielectric constant film by reaction of an organo silane compound and an oxidizing gas at a low RF power level from 20–200 W. The oxidized organo silane film has excellent barrier properties for use as a liner or cap layer adjacent other dielectric layers. The oxidized organo silane film can also be used as an etch stop or an intermetal dielectric layer for fabricating dual damascene structures. The oxidized organo silane films also provide excellent adhesion between different dielectric layers. A preferred oxidized organo silane film is produced by reaction of methyl silane, CH_3SiH_3, and nitrous oxide, N_2O, at a pulsed RF power level from 50–200 W during 10–30% of the duty cycle.

26 Claims, 9 Drawing Sheets



US005817572A

United States Patent [19]

Chiang et al.

[11] Patent Number: 5,817,572

[45] Date of Patent: Oct. 6, 1998

[54] **METHOD FOR FORMING MULTILEVES INTERCONNECTIONS FOR SEMICONDUCTOR FABRICATION**

[75] Inventors: **Chien Chiang**, Fremont; **David B. Fraser**, Danville, both of Calif.

[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[21] Appl. No.: **768,790**

[22] Filed: **Dec. 18, 1996**

Related U.S. Application Data

[63] Continuation of Ser. No. 314,248, Sep. 28, 1994, abandoned, which is a continuation-in-part of Ser. No. 905,473, Jun. 29, 1992, Pat. No. 5,612,254.

[51] **Int. Cl.**[6] **H01L 21/44**

[52] **U.S. Cl.** **438/624**; 438/633; 438/637; 438/671; 438/945; 438/975

[58] **Field of Search** 438/624, 633, 438/637, 671, 945, 975, 700

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Primary Examiner—Caridad Everhart

Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] **ABSTRACT**

A method for forming interconnections for semiconductor fabrication and semiconductor devices have such interconnections are described. A first patterned dielectric layer is formed over a semiconductor substrate and has a first opening filled with conductive material. Another patterned dielectric layer is formed over the first dielectric layer and has a second opening over at least a portion of the conductive material. The first patterned dielectric layer may serve as an etch-stop in patterning the other patterned dielectric layer. Also, a dielectric etch-stop layer may be formed over the first patterned dielectric layer and over the conductive material before the other patterned dielectric layer has been formed. This dielectric etch-stop layer may serve as an etch-stop in patterning the other patterned dielectric layer. The second opening exposes a portion of the dielectric etch-stop layer. The exposed portion of the dielectric etch-stop layer is removed. The second opening is filled with conductive material.

37 Claims, 13 Drawing Sheets